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10/751,525	01/06/2004	Mitsuyasu Ohta	60188-725	3295

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,525	OHTA ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/381377.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/18/04 1/6/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-32 are presented for examination.

Claim Objections

Claims 1, 11, 12, 14, 16, 21-24, 27, 28, and 32 are objected to because of the following informalities: The phrase "characterized by (further) comprising" is unclear and/or redundant. Appropriate correction is required.

Claims 1-24, 27-30, and 32 are objected to because of the following informalities: The noun "integrated circuit" should have an (definite or indefinite) article such as a, an or the. Appropriate correction is required.

Claim 18 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 16 : "... deciding whether the test data received is correct or erroneous, and outputting a result of the decision".

Claim 18: "...on deciding that the test data is erroneous, the decision result output circuit outputs the decision result.".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi U.S. Patent No. 5,930,271.

As per claims 1 and 3, Takahashi teaches the claimed functional block for an integrated circuit with a test data output and a control signal for test mode, with output data that changes from one value to another based on the input data (column 1 lines 23-31, column 6 lines 33-58, figure 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, and 4-9, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi U.S. Patent No. 5,930,271 in view of Koo et al. U.S. Patent No. 5,386,423.

As per claims 2, 4, and 5, Takahashi substantially teaches the claimed functional block for an integrated circuit with a test data output in parallel and a control signal for test mode (column 6 lines 33-58). Not explicitly disclosed is that the output signal lines are grouped and have mutually different values and that the test data will alternately change from one value to another.

However, in an analogous art, Koo et al. teach a test circuit in which outputs can be grouped and a mechanism is shown for setting adjacent latches into logically opposite states. Thus, the expected output is a string of zeroes and ones or ones and zeroes alternating accordingly (column 5 lines 1-10, column 8 lines 3-21). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have combine the testing circuits of Koo et al. and functional blocks of Takahashi. This would have been obvious to one of ordinary skill in the art because as suggested by Koo et al. (column 2 lines 52-65) in order to more easily isolate faults in a circuit.

As per claims 6-9, Takahashi and Koo et al. as combined above, substantially the claimed circuit in which Koo et al. teach a circuit which has a control line that generates and inverts the alternating zero and one signals sent to specific latches where the input to the inverter is tied to selected latches and the output to other specified latches (Koo et al. column 8 lines 7-49).

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. U.S. Patent No. 5,809,039 in view of Luk U.S. Patent No. 6,055,661.

As per claims 16-18, Takahashi et al. substantially teach the claimed integrated circuit divided into a plurality of functional blocks, and an output portion of each functional block is provided with a buffer circuit with a scan function which can change a function of latching data by a control signal and the test data can be entered directly to the buffer or read out of the buffer. Test patterns are generated in each functional block and diagnosis can be carried out in each functional block (column 15 lines 16-30). Not explicitly disclosed is that there is a comparison circuit that provides an output indicating a pass or fail of the test.

However, in an analogous art, Luk teaches a circuit containing a comparator which is connected to a latch controlled by a third programmable time delay. The result of the comparisons made by the comparator is latched into the latch, and pass/fail signal is generated from the latch depending on the result of the comparison made by the comparator (column 7 line 64 through column 8 line 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have included the comparison device of Luk in the testing circuit of Takahashi et al. This would have been obvious because as suggested by Luk, controlling the testing and collecting the response signals for comparison will simplify the testing process (column 3 lines 34-40).

As per claims 19 and 20, Luk teaches storing the results of the comparison in latch circuitry (column 7 line 64 through column 8 line 5).

Claims 23-26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi U.S. Patent No. 5,930,271 in view of Luk U.S. Patent No. 6,055,661.

As per claim 23, Takahashi describes a circuit with multiple functional blocks, a test data output, test control signals for individually accessing or testing the functional blocks and a test control output section for sending the test control signals (column 1 line 60 through column 2 line 67, figure 16). Not explicitly disclosed is that there is a comparison circuit that provides an output indicating a pass or fail of the test.

However, in an analogous art, Luk teaches a circuit containing a comparator which is connected to a latch controlled by a third programmable time delay. The result of the comparisons made by the comparator is latched into the latch, and pass/fail signal is generated from the latch depending on the result of the comparison made by the comparator (column 7 line 64 through column 8 line 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have included the comparison device of Luk in the testing circuit of Takahashi. This would have been obvious as suggested by Takahashi in order to determine whether the tested circuit has passed or failed (column 2 lines 52- 57).

As per claim 24, Takahashi teach input and output signal lines that connect the functional blocks and additional circuits that are storage parts that constitute a mode switching register. The outputs of the storage parts that form the register are connected to respective mode switching terminals of the corresponding functional blocks (column 2 lines 4-26).

As per claims 25 and 26, Luk teaches outputting and displaying the test results (figure 7, column 10 lines 61-63).

As per claim 29, Luk teaches that the results of the comparator are latched into a latching circuit (column 7 lines 64 through column 8 line 7).

Claims 10-15 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi U.S. Patent No. 5,930,271 and Koo et al. U.S. Patent No. 5,386,423 in further view of Negishi U.S. Patent No. 6,119,257.

As per claims 10 and 11, Takahashi and Koo et al. as combined above substantially teach the claimed functional block of an integrated circuit in which Takahashi teaches the claimed functional block for an integrated circuit with a test data output and a control signal for test mode, with output data that changes from one value to another based on the input data (column 1 lines 23-31, column 6 lines 33-58, figure 3). And Koo et al. teach a test circuit in which outputs can be grouped and a mechanism is shown for setting adjacent latches into logically opposite states. Thus, the expected output is a string of zeroes and ones or ones and zeroes alternating accordingly

(column 5 lines 1-10, column 8 lines 3-21). Not explicitly disclosed is that the system contains multiple pattern generators and a decision output circuit.

However in an analogous art Negishi teach multiple pattern generators which are selected using multiplexers, a comparison circuit for comparing test data with expected data, and an output to a memory to store the test results (figure 1, column 5 line 46 through column 6 line30). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method of testing a functional block as taught by Takahashi and Koo et al. with the methods of Negishi. This would have been obvious as suggested by Takahashi in order to enable independent testing of functional blocks (column 1 line 60 through column 2 line 3).

As per claims 12, 14, 21, and 22, Negishi teaches a method of the output being inhibited in response to a control signal (column 9 line 60 through column 10 line 4).

As per claims 13 and 15 Negishi teaches a method of inverting the signal from a pattern generator in response to a reset signal Column 8 line 66 through column 9 line 10 and column 9 lines 48-59).

Double Patenting

Claims 23-32 rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-10 of prior U.S. Patent No. 6,708,301. This is a double patenting rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,108,806 Abramovici et al.

This patent teaches a method of testing field programmable gate arrays (FPGAs) includes establishing a first group of programmable logic blocks as test pattern generators or output response analyzers and a second group of programmable logic blocks as blocks under test . This is followed by generating test patterns and comparing outputs of two blocks under test with one output response analyzer. Next is the combining of results of a plurality of output response analyzers utilizing an iterative comparator in order to produce a pass/fail indication.

Examiner note: The files of this case were searched in order to determine if another set of claims were entered with the preliminary amendment. A new set of claims was not found in the files. As such, since the claims which were examined were identical to the claims submitted n the parent application, the rejections are simuliar.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2117